Transactional Coherence and Consistency on M32R Multiprocessor Platform

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Introduction

- PLUTO: TCC M32R Prototype
- Developing environment

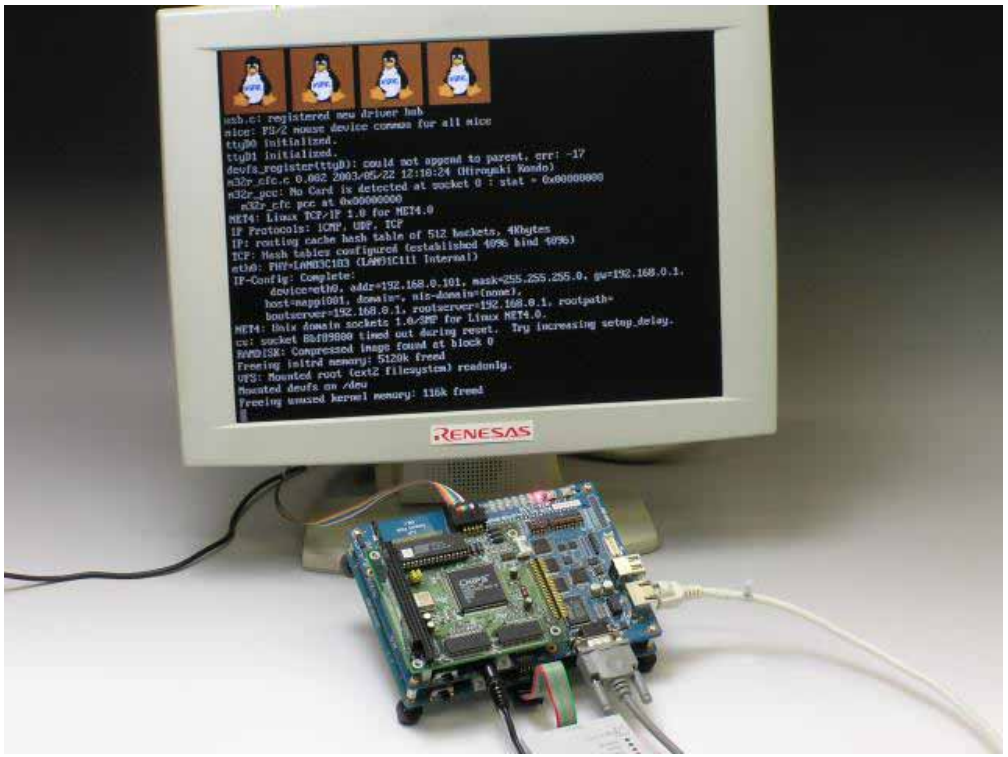
- FPGA-based Multiprocessor Platform.

- Trial Version (TCC specification is based on ATLAS / minimum spec.)

- Hardware: HDL / FPGA mapping
- Software : TCC API

- Programs run on this platform.

M32R Multiprocessor Platform



- M32R Multiprocessor mapped on FPGAs.
- SMP Linux working on this platform.
- Debugging Interface based on JTAG.

M32R microprocessor

- High performance, compact embedded 32bit RISC CPU Core
- M32R Softmacro Core

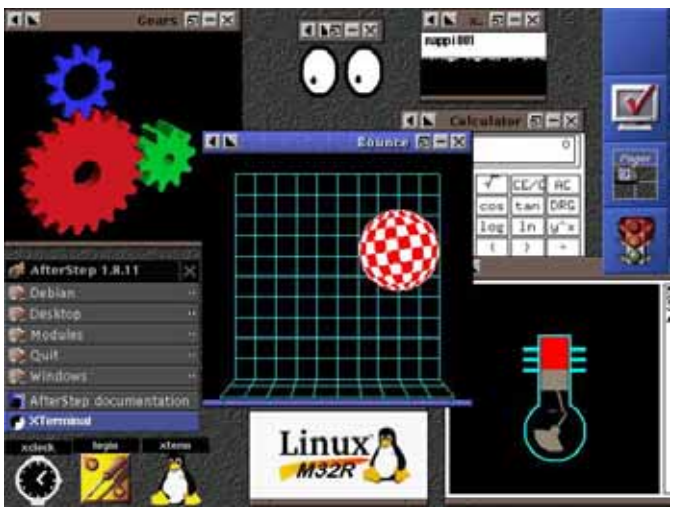
  - is a fully synthesizable core coded by VerilogHDL.
  - can be programmed to FPGAs.
  - provides an efficient platform for supporting processor architecture development.

Software Environment

- Linux/M32R
  - is a Debian Gnu/Linux distribution
  - kernel-2.4.27 , 2.6.14
  - supports SMP features.
  - supports OpenMP, Pthreads

http://www.linux-m32r.org

- Development Environment
  - linux-m32r-gcc 4.0
  - Debugging tool of JTAG-ICE and gdb

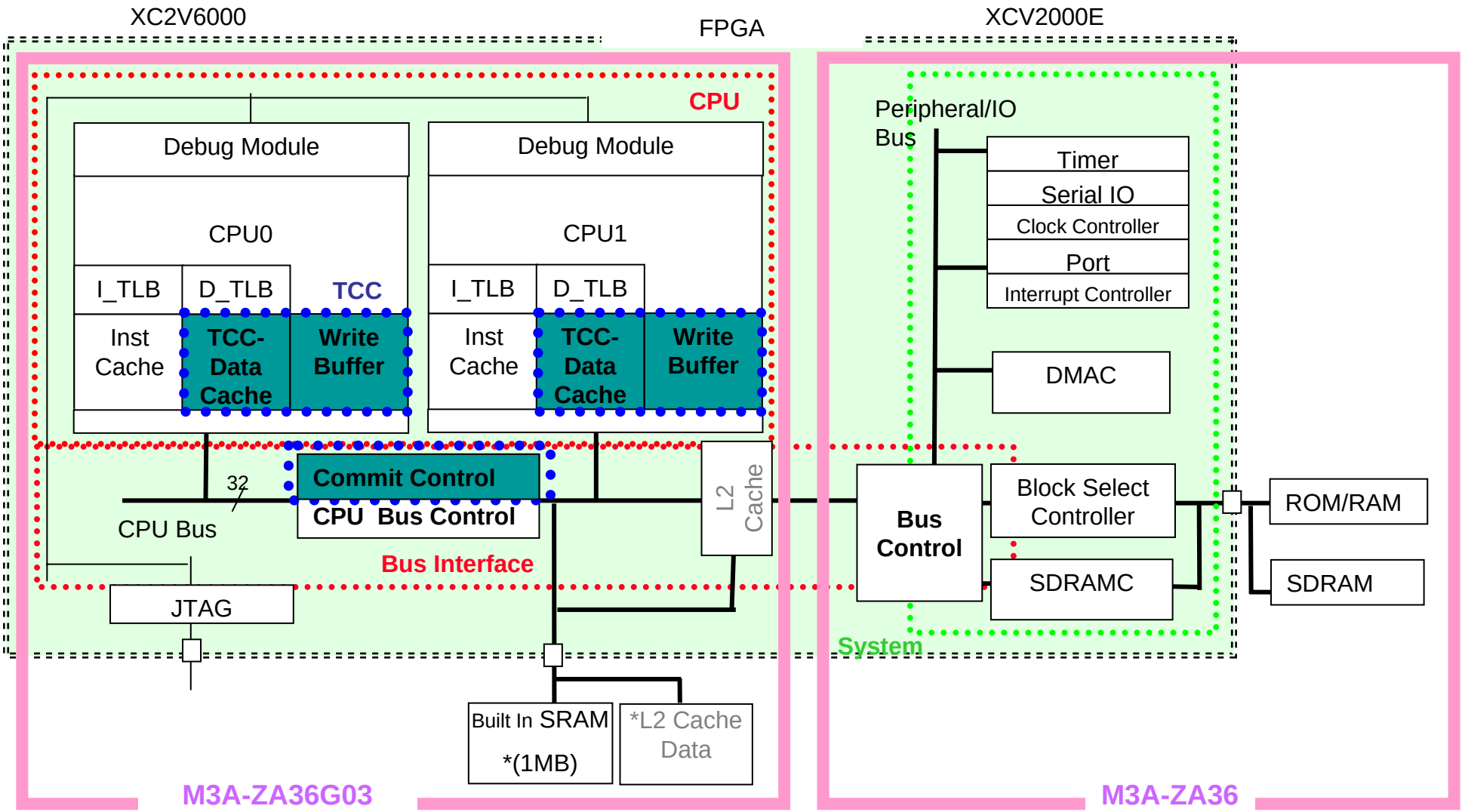


TCC Implementation

- Enhancements for TCC are

- Primary TCC Data Cache
- Bus Arbiter with TCC protocol (Commit, PhaseID Controller)
- CPU Core Architecture with
  - TCC Exception / Interrupt for overflow, violation handling

PLUTO (TCC M32R prototype) Block Diagram



*Built in SRAM and L2 Cache are alternatives. This prototype now supports SRAM only.

Specification (1)

Items		**Spec**
CPU	Core	M32R / 2 CPU
	MMU	ITLB/DTLB 16 entry
Internal Memory	SRAM	1MByte
	Cache Memory	Instruction 8K byte (2way) Data cache 8K byte (2way)
Peripherals	SDRAM controller	2ch (For 64M – 256Mbit SDRAM)
	Multi Function Timer	16bit × 6ch
	DMA Controller	2ch
	Block Select Controller	64M Byte Area × 8Block
	Serial IO	2ch
	Interrupt Controller Unit	7 level,63 factors can be entered
	On chip Debug I/F	Based on JTAG

Specification (2)

Items	Data Cache (Original)	TCC Data Cache
Capacity	8 Kbytes	8 Kbytes
Mapping method	Two-way set associative	Two-way set associative
Replace method	LRU algorithm	**None**
Main memory updating method	Write Back	**TCC method** **Update when commit**
Coherence guarantee	MESI	**TCC method**
Attribute	V (Valid)	**SR (Speculative Read)** **SW (Speculative Write)**
Line Size	128 bits (16bytes)	128 bits (16bytes)
Data Part	16bytes x 256 entries x 2ways = 8Kbytes	16bytes x 256 entries x 2ways = 8Kbytes
Write Buffer	None	**2K Entry with line index and way information**

Conclusions

- PLUTO: TCC M32R Prototype
  provides efficient platform for supporting processor architecture development.

Current work

- Benchmarks
- Operating System (Linux)
- Feedback to TCC Architecture

Links to related pages

- Linux/M32R Home Page http://www.linux-m32r.org
- Renesas Technology Corp. http://www.renesas.com/
- M32R microprocessor
  http://www.renesas.com/eng/products/mpumcu/32bit/m32r/index.html